



HyperTransport Tunnel



PRODUCT BRIEF

Overview Features

High-Speed Low-Latency Point-to-Point Link

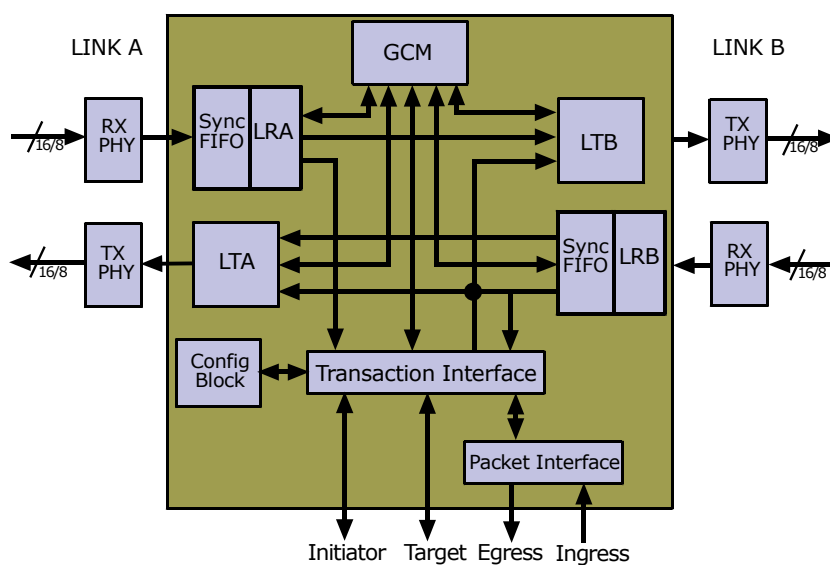
HyperTransport technology is a high-speed, low-latency, point-to-point link for interconnecting integrated circuits (ICs) on a board. It is a packet-based link implemented on two independent uni-directional sets of wires. HyperTransport tunnel is a popular topology with dual HyperTransport links which allows daisy chaining of tunnel devices to create an IO channel, connecting multiple I/O devices to a host system.

GDA's HyperTransport Tunnel core, code named HyperTunnel, is designed for reuse and it's flexible backend interface makes it easy to be integrated into wide range of applications. The core provides highly scalable upstream and downstream bandwidths through programmable link widths and frequencies.

HyperTunnel core meets today's demand for the increased bandwidth and offers more bandwidth than any existing solutions. The upstream link could be run 24 times faster than a 32 bit, 33 MHz PCI bus. The core is designed to operate the upstream link at up to 800 MHz DDR, yielding an effective transfer rate of 1.6 Gbits per second per wire pair. The design targets networking, telecommunications, embedded systems and any application where high speed, low latency response, low pin counts and scalability are necessary.

- Proven design compliant with HyperTransport I/ O Link Specification, Version 1.03
- Provides dual HyperTransport links
- Either link can be hardware configured for 16- bit or 8-bit link interface
- Either link supports software programmable link widths of 16, 8, 4, or 2bits.
- Either link can be configured as upstream
- Either link supports 800, 600, 500, 400, or 200 MHz link frequency
- Maximum bandwidth is 6.4 GB/sec on both links
- Supports independent link width and frequency for each link
- Supports link disconnect protocol
- Supports interrupt
- Supports external and internal loop backs on both HyperTransport links
- Optional transaction interface provides target and initiator interfaces
- Optional packet interface for network applications

HT Tunnel Core



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HyperTransport Tunnel

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Specifications

Configurable Options

- Link Widths: 16/8 bits
- Back-end interface can be configured to transaction interface or packet interface mode
- Transaction interface can be configured to support target interface only
- Configurable buffer size for each virtual channel

Design Attributes

- Highly modular design
- Fully synchronous, technology-independent design
- 128-bit wide internal data path
- Most part of the Tunnel logic operates at 200 MHz core clock
- Clearly demarked clock domains
- Active-low asynchronous reset

Product Package

- RTL code
- Detailed design document
- Verification environment
- Test cases
- Synthesis environment/scripts

Documentation

- User manual
- Verification guide
- Synthesis guide

Status : Gold [silicon proven]
Availability : April 2002
Language : Verilog HDL
Synthesis : Design Compiler
Simulation : Verilog-XL/NC, VCS
Technology : 0.18u Standard Cell

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