



HyperTransport Host



PRODUCT BRIEF

Overview Features

High-Speed Low-Latency Point-to-Point Link

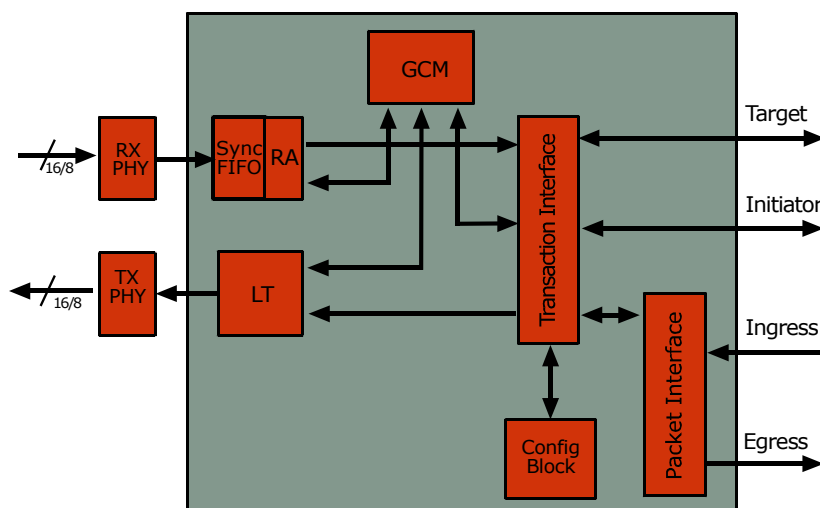
HyperTransport technology is a high-speed, low-latency, point-to-point link for interconnecting integrated circuits (ICs) on a board. It is a packet-based link implemented on two independent uni-directional sets of wires. HyperTransport Host is the root of the HyperTransport fabric.

GDA's HyperTransport Host core, code named HyperHost, is designed for reuse and its flexible backend interface makes it easy to be integrated into wide range of applications. The core provides highly scalable bandwidth through programmable link widths and frequencies.

HyperHost core meets today's demand for the increased bandwidth and offers more bandwidth than any existing solutions. The core could be run 24 times faster than a 32 bit, 33 MHz PCI bus. The core is designed to operate the link at up to 800 MHz DDR, yielding an effective transfer rate of 1.6 Gbits per second per wire pair. The design targets networking, telecommunications, embedded systems and any application where high speed, low latency response, low pin counts and scalability are necessary.

- Compliant with HyperTransport I/O Link Specification, Ver. 1.03
- Can be hardware configured for 16-bit or 8-bit link interface
- Supports software programmable link widths of 16, 8, 4 or 2 bits
- Supports 800, 600, 500, 400, or 200 MHz link frequency
- Maximum bandwidth is 6.4 Gb/sec
- Supports double-hosted chain
- Supports link disconnect protocol
- Supports peer-to-peer transactions
- Supports reset generation
- Supports interrupt
- Supports external and internal loop backs
- Optional transaction interface provides target and initiator interfaces
- Optional packet interface for network applications

HT Host Core





HyperTransport Host

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Specifications

Configurable Options

- Link Widths: 16/8 bits
- Back-end interface can be configured to transaction interface or packet interface mode
- Transaction interface can be configured to support target interface only
- Configurable buffer size for each virtual channel

Design Attributes

- Highly modular design
- Fully synchronous, technology-independent design
- 128-bit wide internal data path
- Most part of the Host logic operates at 200 MHz core clock
- Clearly demarked clock domains
- Active-low asynchronous reset

Product Package

- RTL code
- Detailed design document
- Verification environment
- Test cases
- Synthesis environment/scripts

Documentation

- User manual
- Verification guide
- Synthesis guide

Status : Bronze [under development]

Availability : June 2002

Language : Verilog HDL

Synthesis : Design Compiler

Simulation : Verilog-XL/NC, VCS

Technology : 0.18u Standard Cell

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